

Notice of Allowability

Application No.

09/987,409

Examiner

Lisa Kilday

Applicant(s)

SAKURAI, KAZUNORI

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to after-final amendment of 8/18/4.
2. ☒ The allowed claim(s) is/are 2,3,5,8 and 19-21.
3. ☒ The drawings filed on 14 November 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |

Allowable Subject Matter

Claims 2-3, 5, 8 and 19-21 allowed.

The following is an examiner's statement of reasons for allowance: amendment to independent claim 19 necessitates allowance of claims 2-3, 5, 8 and 19-21. In re claims 2-3, 5, 8 and 19-21, Tsukahara teaches a method of manufacturing a semiconductor device including a step of mounting a semiconductor chip on a wiring substrate having a base substrate (see fig. 14c where the base substrate 21 is pad of the wiring substrate which comprises references 4 + 21) on which are formed interconnecting lines (see ref. 33 in fig. 14b where ref. 33 is part of the interconnecting lines found on the wiring substrate), the method comprising: mounting the semiconductor chip (1) on the base substrate (the area on top near the chip) to that a surface of the base substrate opposite to the surface on which the interconnecting lines (the lines are formed on the bottom of ref. 21 at the interface with ref. 4) are formed with bumps (see ref. 15 in fig. 14b where the bumps are down and touch the contact surface and in fig. 14c where the bumps penetrate the substrate and contact is with the base substrate) formed on the semiconductor chip (1). Prior art fails to teach or suggest the limitation of: pushing the bumps into the base substrate from the first surface through the base substrate to a second surface opposite to the first surface and then electrically connecting the bumps to interconnecting lines formed on the second surface of the base substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

Art Unit: 2829

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion


Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (571) 272-1962. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar, can be reached on (571) 272-1812. The fax number for the group is (703) 872-9306. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

LAK

9/2/04


Michael Tokar
Supervisory Patent Examiner
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